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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,313	04/13/2004	Zhenjiang Cui	007034 USAP03/DSM/BCVD/J	5975

7590 05/11/2005

APPLIED MATERIALS, INC.
PATENT COUNSEL, MS/2061
Legal Affairs Department
P.O. BOX 450A
Santa Clara, CA 95052

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,313	CUI ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Objections

Claim 9 is objected to because of the following informalities:

In independent claim 9, line 9, after "implanting to form", delete "course" and insert --source--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ross (U.S. Patent 6,548,899) in view of Lee et al. (U.S. Patent 6,664,172).

In re claim 1, **Ross** discloses a method for treating a silicon nitride (Si_xN_y) film, the method comprising: forming the silicon nitride film; and electron beam treating the silicon nitride film with a sufficiently high electron dosage (col. 2, lines 55-65 and col. 5, line 54 to col. 6, line 42).

> On the surface of the substrate is an optional pattern of raised lines, such as metal, oxide, nitride or oxynitride lines which are formed by well known lithographic techniques. Suitable materials for the lines include silica, silicon nitride, titanium nitride, tantalum nitride, aluminum, aluminum alloys, copper, copper alloys, tantalum, tungsten and silicon oxynitride. These lines form the conductors or insulators of an integrated circuit. Such are typically closely separated from one another at distances of about 20 micrometers or less, preferably 1 micrometer or less, and more preferably from about 0.05 to about 1 micrometer.

> The film may also be cured by exposing the surface of the substrate to a flux of electrons. Whether the film is cured by electron beam exposure or is cured by other means such as heating or exposure to UV light, the surface of the dielectric film is exposed to sufficient electron beam exposure to remove substantially all moisture and contaminants from the surface of the dielectric layer.

Ross does not explicitly disclose treating the silicon nitride film with a sufficient high electron dosage to reduce a H content of the silicon nitride film.

Lee, however, discloses forming a silicon nitride layer Si_3N_4 and performing a dehydrogenation process on the silicon nitride layer (col. 7, claim 13).

> 12. The method of claim 9 wherein the conductive line comprises a bit line or a word line.
> 13. A method of making a metal-oxide-semiconductor (MOS) transistor with improved threshold voltage (V_t) stability, the method comprising:
> providing a semiconductor substrate;
> forming the gate of at least one transistor on a surface of the semiconductor substrate, the gate comprising a gate oxide layer and a conductive layer;
> forming a lightly doped drain (LDD) of the transistor;
> forming a silicon nitride layer Si_3N_4 layer) on a surface of the gate of the transistor and the semiconductor substrate by performing a low thermal budget process;
> performing a dehydrogenation process on the silicon nitride layer;
> etching the silicon nitride layer to form a spacer in the periphery of the gate, and
> forming a source/drain (S/D) of the transistor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Ross and Lee to enable the process of treating the silicon nitride film with a sufficiently high electron dosage to reduce a H content of the silicon nitride film of Ross to be performed and furthermore to improve the stability of threshold voltage (col. 3, lines 27-32, Lee et al.).

In re claim 2, **Ross** discloses that the method of claim 1, which further comprises heating the film to a temperature in a range from about 25° C to about 1050° C (col. 5, line 61 to col. 6, line 11).

> Preferably the electron beam exposure is done at a vacuum in the range of from about 10^{-5} to about 10^{2} torr, and with a substrate temperature in the range of from about 25° C. to about 1050° C. When the electron beam is used both for

In re claim 3, **Ross** discloses that the step of electron beam treating includes exposing the film to electron beam current at doses in a range from about 100 $\mu C/cm^2$ to about 5,000 $\mu C/cm^2$ (col. 6, lines 12-21).

> When the electron beam is used both for dielectric curing and surface treatment, the electron beam dose will fall into the range of from about 1 to about 100,000 $\mu C/cm^2$, preferably from about 100 to about 10,000$\mu C/cm^2$, and more preferably from about 1 to about 8,000 $\mu C/cm^2$. The dose and energy selected will be proportional to the thickness of the films to be processed. When the electron beam is used as a dielectric surface treatment, energy and doses will fall into the ranges of about 0.5 to about 3 KeV and about 100 to about 5,000 $\mu C/cm^2$, respectively. The appropriate doses and

In re claim 4, **Ross** discloses that the step of electron beam treating further includes exposing the film from about 0.5 minute to about 120 minutes (col. 6, lines 12-42).

> about 1000 Å from the surface. Generally the exposure will range from about 0.5 minute to about 120 minutes, and preferably from about 1 minute to about 60 minutes. The

In re claim 5, **Ross** discloses that the step of electron beam treating comprises placing the film in an ambient gas in a chamber wherein the electron beam is formed between a cathode and an anode, and providing a cathode voltage in range form about -.5 KV to about –10 KV (col. 6, lines 12-42).

In re claim 6, **Ross** discloses wherein the ambient gas is one or more of N_2, H_2, Ar, O_2, or any combination of these gases (col. 6, lines 40-42).

40 inches. The gaseous ambient in the electron beam system chamber may be nitrogen, hydrogen, argon, oxygen, or any combinations of these gases.

In re claim 7, **Ross** discloses that a pressure of the ambient gas in the chamber and a working distance between the cathode and the anode are maintained so that arcing does not occur between the cathode and the anode (col. 7, line 28 to col. 8, line 7).

In re claim 8, **Ross** discloses wherein the pressure of the ambient gas in the chamber is maintained at one or more levels that provide a substantially constant electron beam current during at least one treatment period (col. 7, lines 28 to col. 8, line 7).

2. Claims 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. Patent 6,664,172) in view of Ross (U.S. Patent 6,548,899).

In re claim 9, **Lee** discloses a method for fabricating a pMOSFET, the method comprising: oxidizing a gate; forming a gate electrode **108, 114** (col. 4, lines 19-43 and FIG. 7);

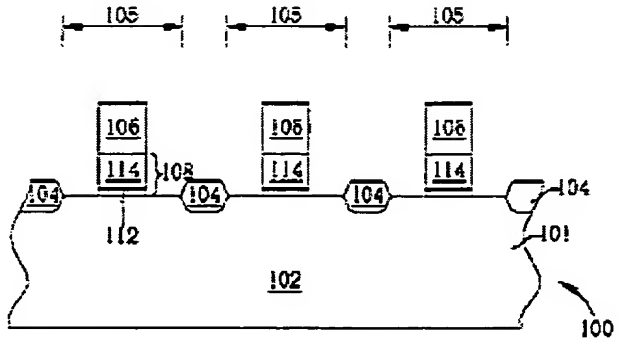

Fig. 7

implanting to form shallow source/drain extensions **116** (col. 4, lines 44-57 and FIG. 8);

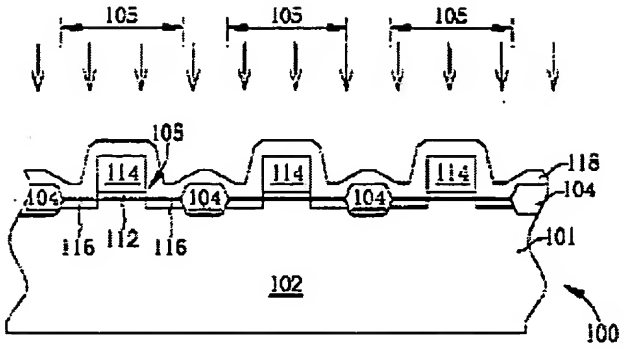

Fig. 8

forming a SiN gate sidewall **118** (col. 4, lines 44-57);

treating the SiN gate sidewall with a sufficiently high electron dosage to reduce a H content of the silicon nitride film (col. 7, claim 13);

12. The method of claim 9 wherein the conductive line comprises a bit line or a word line.

13. A method of making a metal-oxide-semiconductor (MOS) transistor with improved threshold voltage (V_t) stability, the method comprising:

providing a semiconductor substrate;

forming the gate of at least one transistor on a surface of the semiconductor substrate, the gate comprising a gate oxide layer and a conductive layer;

forming a lightly doped drain (LDD) of the transistor;

forming a silicon nitride layer (Si_3N_4 layer) on a surface of the gate of the transistor and the semiconductor substrate by performing a low thermal budget process;

performing a dehydrogenation process on the silicon nitride layer;

etching the silicon nitride layer to form a spacer in the periphery of the gate, and

forming a source/drain (S/D) of the transistor.

implanting to form source/drain deep junctions **124, 126**; and activating the source/drain (col. 5, lines 29-36 and FIG. 10).

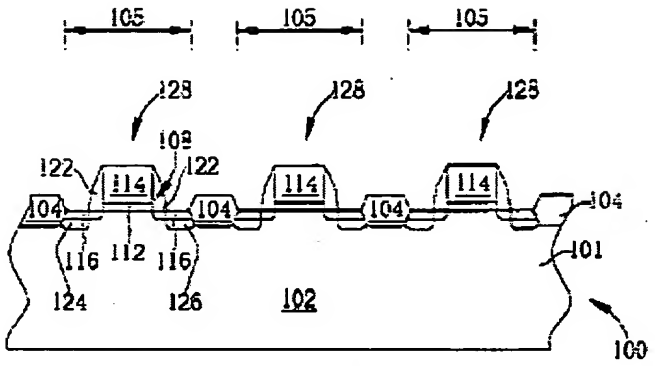

Fig. 10

Lee does not explicitly disclose electron beam treating the SiN gate sidewall with a sufficiently high electron dosage as recited in the Applicants' claimed invention.

Ross, however, discloses electron beam treating the silicon nitride film with a sufficiently high electron dosage (col. 2, lines 55-65 and col. 5, line 54 to col. 6, line 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Lee and Ross to enable the process of treating the silicon nitride film with a sufficiently high electron dosage to reduce a H content of the silicon nitride film of Lee to be performed and furthermore to remove substantially all moisture and contaminants form the surface of the layer (col. 5, lines 54-60, Ross).

In re claim 10, **Ross** discloses that the step of electron beam treating includes heating the SiN gate sidewall to a temperature in a range from about 25° C to about 1050° C (col. 5, line 61 to col. 6, line 11).

> Preferably the electron beam exposure is done at a vacuum in the range of from about 10^{-5} to about 10^{2} torr, and with a substrate temperature in the range of from about 25° C. to about 1050° C. When the electron beam is used both for

In re claim 11, **Ross** discloses that the step of electron beam treating includes exposing the SiN gate sidewall to electron beam current at doses in a range from about 100 $\mu C/cm^2$ to about 5,000 $\mu C/cm^2$ (col. 6, lines 12-21).

> When the electron beam is used both for dielectric curing and surface treatment, the electron beam dose will fall into the range of from about 1 to about 100,000 $\mu C/cm^2$, preferably from about 100 to about 10,000$\mu C/cm^2$, and more preferably from about 1 to about 8,000 $\mu C/cm^2$. The dose and energy selected will be proportional to the thickness of the films to be processed. When the electron beam is used as a dielectric surface treatment, energy and doses will fall into the ranges of about 0.5 to about 3 KeV and about 100 to about 5,000 $\mu C/cm^2$, respectively. The appropriate doses and

In re claim 12, **Ross** discloses that the step of electron beam treating includes exposing the SiN gate sidewall from about 0.5 minute to about 120 minutes (col. 6, lines 12-42).

> about 1000 Å from the surface. Generally the exposure will range from about 0.5 minute to about 120 minutes, and preferably from about 1 minute to about 60 minutes. The

In re claim 13, **Ross** discloses that the step of electron beam treating comprises placing the SiN gate sidewall in an ambient gas in a chamber wherein an electron beam is formed between a cathode and an anode, and providing a cathode voltage in range form about -.5 KV to about –10 KV (col. 6, lines 12-42).

In re claim 14, **Ross** discloses that the ambient gas is one or more of N_2, H_2, Ar, O_2, or any combination of these gases (col. 6, lines 40-42).

> inches. The gaseous ambient in the electron beam system chamber may be nitrogen, hydrogen, argon, oxygen, or any combinations of these gases.

In re claim 15, **Ross** discloses that a pressure of the ambient gas in the chamber and a working distance between the cathode and the anode are maintained so that arcing does not occur between the cathode and the anode (col. 7, line 28 to col. 8, line 7).

In re claim 16, **Ross** discloses that the pressure of the ambient gas in the chamber is maintained at one or more levels that provide a substantially constant electron beam current during at least one treatment period (col. 7, lines 28 to col. 8, line 7).

I n re claims 17 and 18, **Lee** in combination with Ross inherently reduce a H content of the silicon nitride film through substantially the entire thickness of the silicon nitride film.

3. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ross (U.S. Patent 6,548,899) in view of Lee et al. (U.S. Patent 6,664,172).

In re claim 19, **Ross** discloses a method for treating a silicon nitride (Si_xN_y) film, the method comprising: forming the silicon nitride film having a thickness; and electron beam treating the silicon nitride film with a sufficiently high electron dosage (col. 2, lines 55-65 and col. 5, line 54 to col. 6, line 42).

> On the surface of the substrate is an optional pattern of raised lines, such as metal, oxide, nitride or oxynitride lines which are formed by well known lithographic techniques. Suitable materials for the lines include silica, silicon nitride, titanium nitride, tantalum nitride, aluminum, aluminum alloys, copper, copper alloys, tantalum, tungsten and silicon oxynitride. These lines form the conductors or insulators of an integrated circuit. Such are typically closely separated from one another at distances of about 20 micrometers or less, preferably 1 micrometer or less, and more preferably from about 0.05 to about 1 micrometer.

> The film may also be cured by exposing the surface of the substrate to a flux of electrons. Whether the film is cured by electron beam exposure or is cured by other means such as heating or exposure to UV light, the surface of the dielectric film is exposed to sufficient electron beam exposure to remove substantially all moisture and contaminants from the surface of the dielectric layer.

Ross does not explicitly disclose treating the silicon nitride film with a sufficient high electron dosage to reduce the H content of the silicon nitride film through substantially the entire thickness of the silicon nitride film.

Lee, however, discloses forming a silicon nitride layer Si_3N_4 and performing a dehydrogenation process on the silicon nitride layer (col. 7, claim 13).

> 12. The method of claim 9 wherein the conductive line comprises a bit line or a word line.
>
> 13. A method of making a metal-oxide-semiconductor (MOS) transistor with improved threshold voltage (V_t) stability, the method comprising:
>
> providing a semiconductor substrate;
>
> forming the gate of at least one transistor on a surface of the semiconductor substrate, the gate comprising a gate oxide layer and a conductive layer;
>
> forming a lightly doped drain (LDD) of the transistor;
>
> forming a silicon nitride layer Si_3N_4 layer) on a surface of the gate of the transistor and the semiconductor substrate by performing a low thermal budget process;
>
> performing a dehydrogenation process on the silicon nitride layer;
>
> etching the silicon nitride layer to form a spacer in the periphery of the gate, and
>
> forming a source/drain (S/D) of the transistor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Ross and Lee to enable the process of treating the silicon nitride film with a sufficiently high electron dosage to reduce the H content of the silicon nitride film through substantially the entire thickness of the silicon nitride film of Ross to be performed and furthermore to improve the stability of threshold voltage (col. 3, lines 27-32, Lee et al.).

In re claim 20, **Ross** discloses that the step of electron beam treating includes exposing the film to electron beam current at doses in a range from about 100 $\mu C/cm^2$ to about 5,000 $\mu C/cm^2$ (col. 6, lines 12-21).

> When the electron beam is used both for dielectric curing and surface treatment, the electron beam dose will fall into the range of from about 1 to about 100,000 $\mu C/cm^2$, preferably from about 100 to about 10,000$\mu C/cm^2$, and more preferably from about 1 to about 8,000 $\mu C/cm^2$. The dose and energy selected will be proportional to the thickness of the films to be processed. When the electron beam is used as a dielectric surface treatment, energy and doses will fall into the ranges of about 0.5 to about 3 KeV and about 100 to about 5,000 $\mu C/cm^2$, respectively. The appropriate doses and

Response to Applicant's Amendment and Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Applicants contend that Ross et al. does not teach a method for treating a silicon nitride film to reduce a H content in the film by forming a silicon nitride film and electron beam treating the silicon nitride film at a sufficiently high electron dosage to reduce a H content in the silicon nitride film.

In response to Applicants' contention that Ross et al. does not teach a method for treating a silicon nitride film to reduce a H content in the film by forming a silicon nitride film and electron beam treating the silicon nitride film at a sufficiently high electron dosage to reduce a H content in the silicon nitride film, Examiner respectfully disagrees. Since the Applicants' amendment necessitated the new ground(s) of rejection presented in this Office Action, Applicants' argument is moot. Examiner respectfully submits that the newly discovered reference, Lee et al. (U.S. Patent 6,664,172) in combination with

Ross (U.S. Patent 6,548,899) disclose the Applicants' claimed invention (see the rejection presented in this Office Action, on pages 2-3).

For this reason, Examiner holds the rejection proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
May 09th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER